PATENT
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Customer No. 24,118

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPLICANT:	RAHUL MEHRA BRENDAN LYNSKEY	)
SERIAL NO.:	09/802,021	)
FILED:	MARCH 8, 2001	)
FOR:	CONTROL SYSTEM FOR STORAGE MEANS	)
GROUP ART UNIT: 2621		)
EXAMINER:	JAMIE JO ATALA	)

APPELLANTS' REPLY BRIEF

Mail Stop – Board of Patent
Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants/Appellants, Rahul Mehra and Brendan Lynskey, file this Reply Brief pursuant to 37 CFR §41.41 in support of their appeal to the Board of Patent Appeals and Interferences.

This Reply Brief does not contain any new or non-admitted amendment, affidavit or other evidence.

Status of the Claims

Claims 4 through 11, 13 through 15, 17 and 18 are pending in the present patent application and are appealed herein. Claim 18 is an independent claim relating to a receiver for digital data broadcast from a remote location. Claims 4, 5, 9, 15, and 17 each depend on Claim 18. Claim 6 is dependent on Claim 4, Claim 7 is dependent on Claim 6, Claim 8 is dependent on Claim 7, Claim 10 is dependent on Claim 9, Claim 11 is dependent on Claim 10, Claim 13 is dependent of Claim 7, and Claim 14 is dependent on Claim 9.

In summary, Claims 1, 2, 3, 12 and 16 have been cancelled, Claims 4 through 11, 13 through 15, 17 and 18 are pending, rejected, and on appeal. No claims have been allowed to date.

Grounds of Rejection

The grounds of rejection to be reviewed on appeal are as follows:

Are Claims 4 through 11, 13 through 15, 17 and 18 unpatentable under 35 U.S.C. §103(a) over Schindler et al. (U.S. Patent No. 5,995,155) in view of Brightman et al. (U.S. Patent Publication No. 2006/0292292) in view of Stoney (U.S. Patent No. 6,237,079)?

Argument

With respect to the Examiner`s reliance on Schindler et al, the Examiner on page 13 of the Examiner's Brief states that Schindler discloses at column 11, lines 10-67 that the FIFO buffer receives information that is "both MPEG data that has been buffered as well as control commands provided from the user and the system" (underlining added). Schindler et al at column 11, lines 10-67 provides as follows:

When the MPEG data is buffered, a FIFO type of buffer is used, with new information written over the oldest information when the buffer is full. Through use of the television and VCR remote controls on handheld remote 124 and keyboard 126, VCR-like instant replay functions are provided from the buffered MPEG data. The buffered data is sent back under processor 310 control via the PCI bus 312 to the VGA card 318 for display on monitor 122.

The VGA card 318 is now described with reference to FIG. 5. In FIG. 5, a controller 510 is coupled to the PCI bus to receive MPEG encoded video, and other normal personal computer display information such as graphics and text. If controller 510 detects MPEG data on PCI bus 312, it routes it to a decoder 512 with associated dynamic random access memory of 2 megabytes, DRAM 514. Decoder 512 decodes the MPEG data in accordance with MPEG standards. A commercially available chip from SGS-Thompson Microelectronics, part number STi3520 is one such decompressor chip which performs the decompression. DRAM 514 is used as a buffer to assist in the decoding, since large amounts of data are required at one time to decode MPEG data. Audio information from the decoded MPEG data is provided to a header 516 for transmission to the sound card 320. The decoded video signal in YUV color encoding is provided back to controller 510 which then places the video information into a dynamic random access memory or video random access memory, VRAM 518. A converter 520 retrieves the information from VRAM 518 and generates standard analog VGA display signals on a cable adapter 522 which mates with shell 210 in FIG. 2 for display.

Other audio video inputs are provided on VGA card 318, including a standard cable connector at 524 coupled to a video tuner circuit 526. Tuner 526 provides both an audio output on line 528 to header 516, and an audio video signal to a video decoder 530 via line 532. Line 532 is also coupled to a video multiplexer 540, which selects one of at least two NTSC compatible audio video signals it receives to an audio video out panel connector 542. Video decoder 530 also receives audio video inputs from further panel connectors, comprising RCA jack 544, S-video pin 546 and a second RCA jack 548. The video signals provided on these lines are decoded by decoder 530 into YUV video output on line 550, which also receives decoded MPEG signals from decoder 512. Both these signals are available for display by VGA display via controller 510 without conversion to NTSC. An alternative is to route the signals on line 550 to a YUV to NTSC converter 552, which feeds video multiplexer 540 for display on a standard television of NTSC signals. However, conversion to NTSC results in an inferior picture being generated from what is received in either S-video or from the antenna 114 as represented by the MPEG signals on PCI bus 312. By not converting to NTSC, the entire transmitted image may be displayed. Prior art NTSC conversion lead to a cropping of the image to ensure that the image presented was not degraded at the edges. The present invention provides the ability to scale for provision of the entire transmitted image without quality loss at the edges, since it provides a digital video signal. No overscan is required as is needed to ensure smooth display borders for NTSC analog transmissions.

The text relied on only describes buffering MPEG data within the FIFO buffer, rather than the additional claim limitation of intermixing different command types therein. The Examiner has not identified any wording relied upon to justify the assertion that the FIFO buffer receives both MPEG data and also control commands. Indeed, the assertion in the Examiner's Brief contradicts his statements concerning this feature in earlier office actions. Accordingly, the objection is not only incorrect but should be retracted.

Second, the Examiner states on page 13 of the Examiner's Brief that Brightman "is being used to teach the ability to intermix read/write commands on the buffer." The Examiner, however, appears to have misinterpreted Applicants' argument which is that there is no teaching in Brightman of 1) control commands from the control system being intermixed with 2) register read and write commands. As set forth previously, it is explicitly stated at paragraph 485, lines 1-6 of Brightman that the different command types are handled by different FIFO's and are therefore not intermixed as set forth in Claim 18. Brightman, therefore, not only does not disclose or teach the claimed invention but teaches away from the claimed invention and accordingly should be retracted in connection with the rejection.

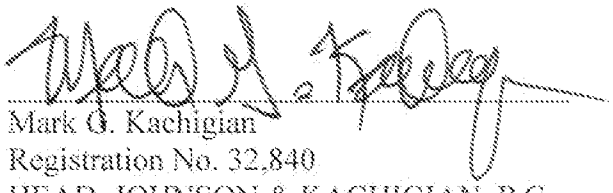
Finally, there is no disclosure in Stoney of intermixing different command types in the same FIFO buffer. Indeed, Stoney teaches away from the present invention by describing how multiple ports are provided with a FIFO buffer for each port, each buffer being dedicated to a particular command type (column 111, lines 48-56). Therefore, the commands in Stoney are not intermixed as set forth in independent Claim 18. Stoney, therefore, not only does not teach or disclose the claimed invention, but teaches away therefrom.

Summary

For all the foregoing reasons, it is believed that the present rejections should be lifted and that the application should proceed to allowance.

The Commissioner is hereby authorized to charge and/or credit any additional fees which may be required to Deposit Account No. 08-1500.

Respectfully submitted,



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